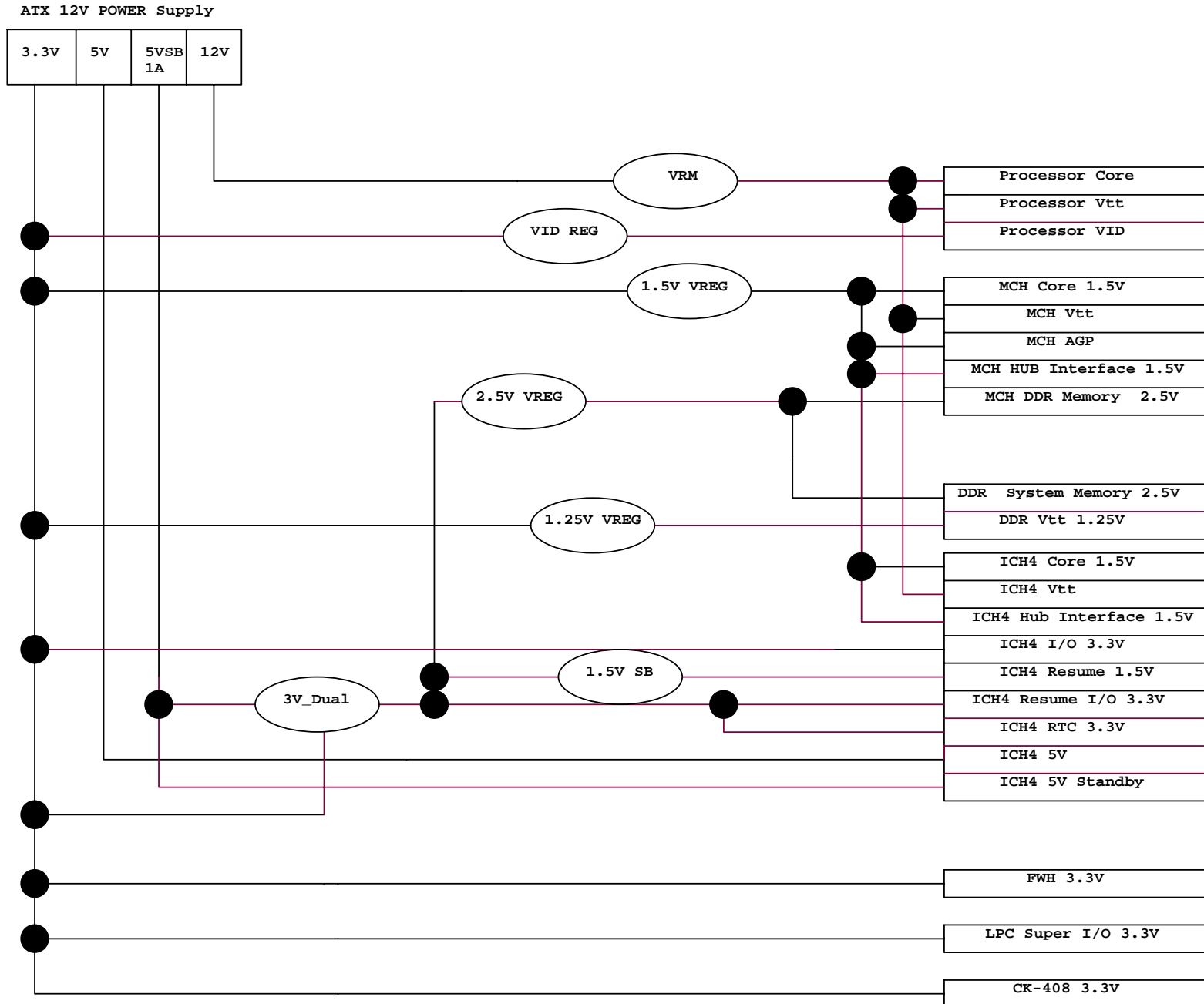


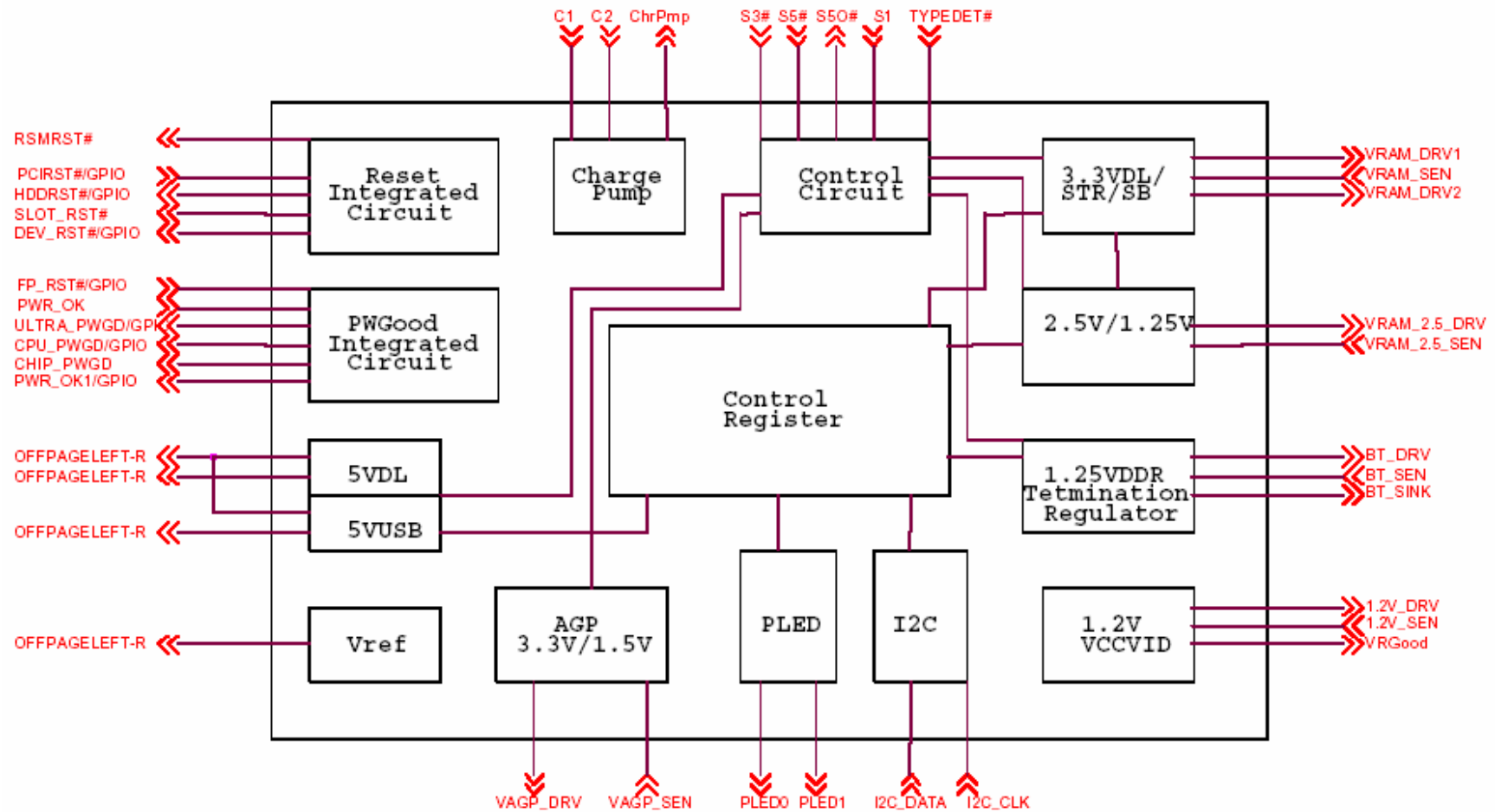
MS-5

**ACPI Controller**

# Intel 845 chipset platform power delivery map



# MS-5 Block Diagram

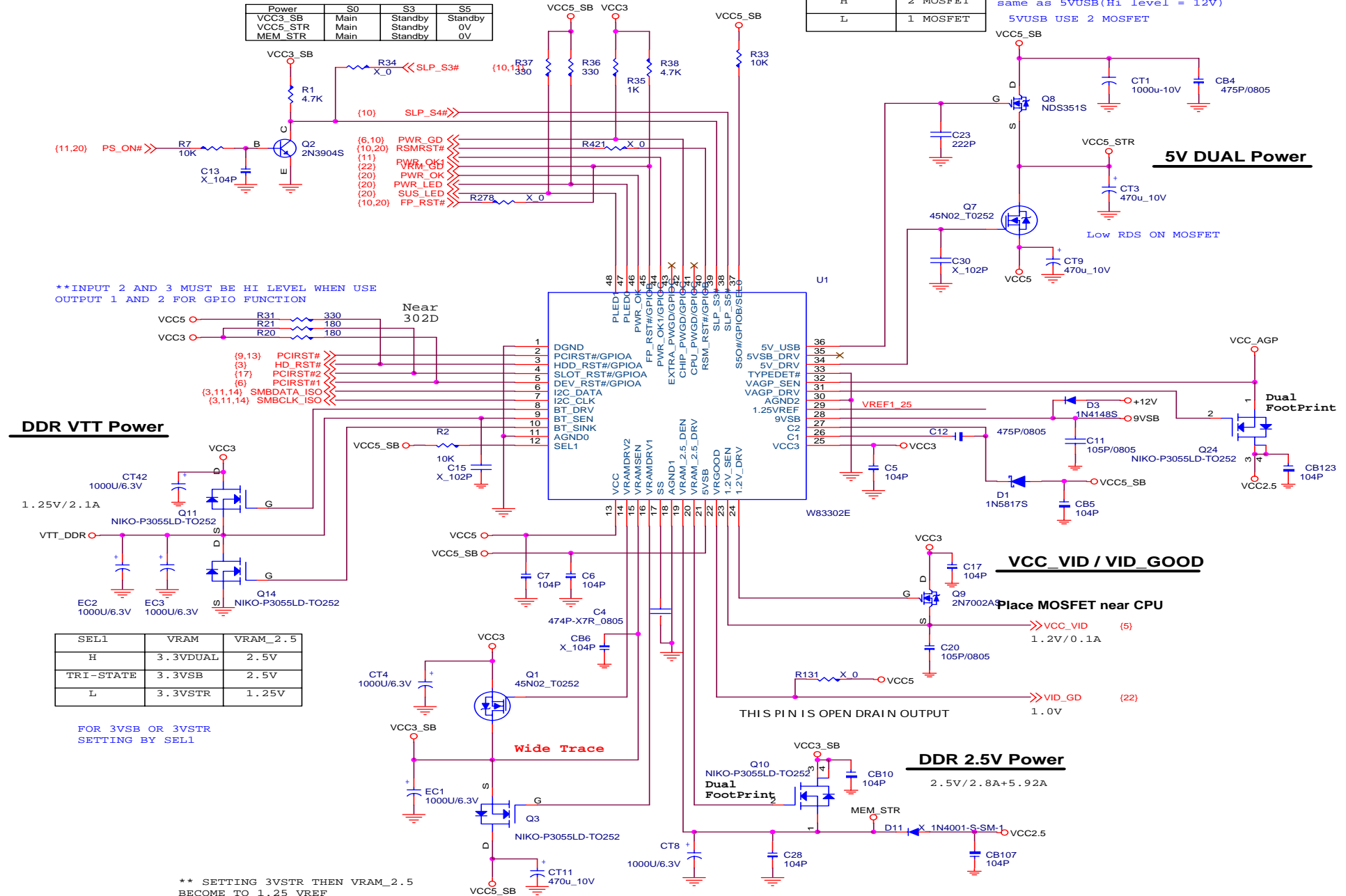


# MS-5 Circuit

Power	S0	S3	S5
VCC3_SB	Main	Standby	Standby
VCC5_STR	Main	Standby	0V
MEM_STR	Main	Standby	0V

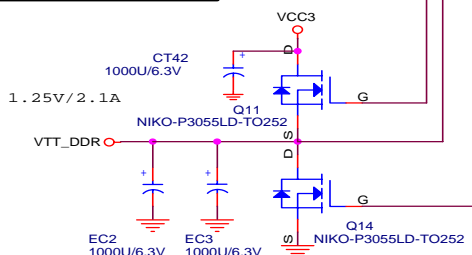
SEL0	5VUSB
H	2 MOSFET
L	1 MOSFET

\*\*S50# pin function(Hi level = 5V)  
same as 5VUSB(Hi level = 12V)  
5VUSB USE 2 MOSFET



\*\*INPUT 2 AND 3 MUST BE HI LEVEL WHEN USE OUTPUT 1 AND 2 FOR GPIO FUNCTION

## DDR VTT Power

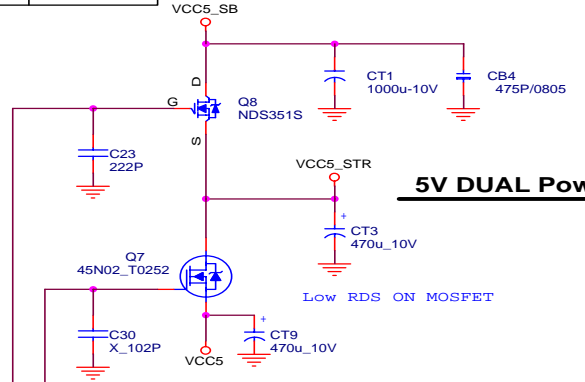


SEL1	VRAM	VRAM_2.5
H	3.3VDUAL	2.5V
TRI-STATE	3.3VSB	2.5V
L	3.3VSTR	1.25V

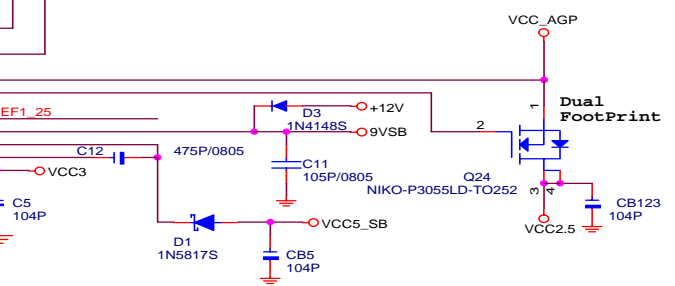
FOR 3VSB OR 3VSTR SETTING BY SEL1

\*\* SETTING 3VSTR THEN VRAM\_2.5 BECOME TO 1.25 VREF

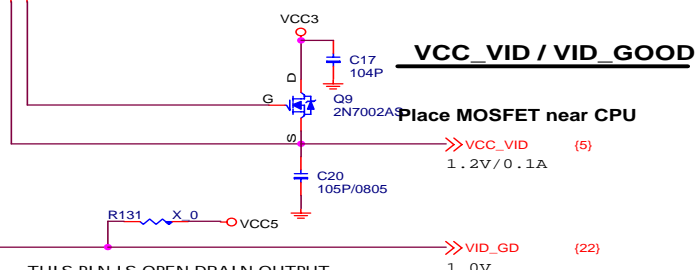
## 5V DUAL Power



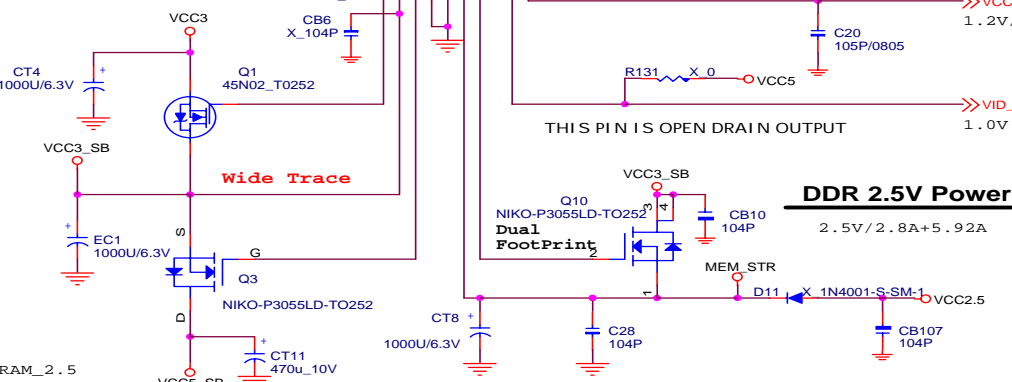
## Dual FootPrint



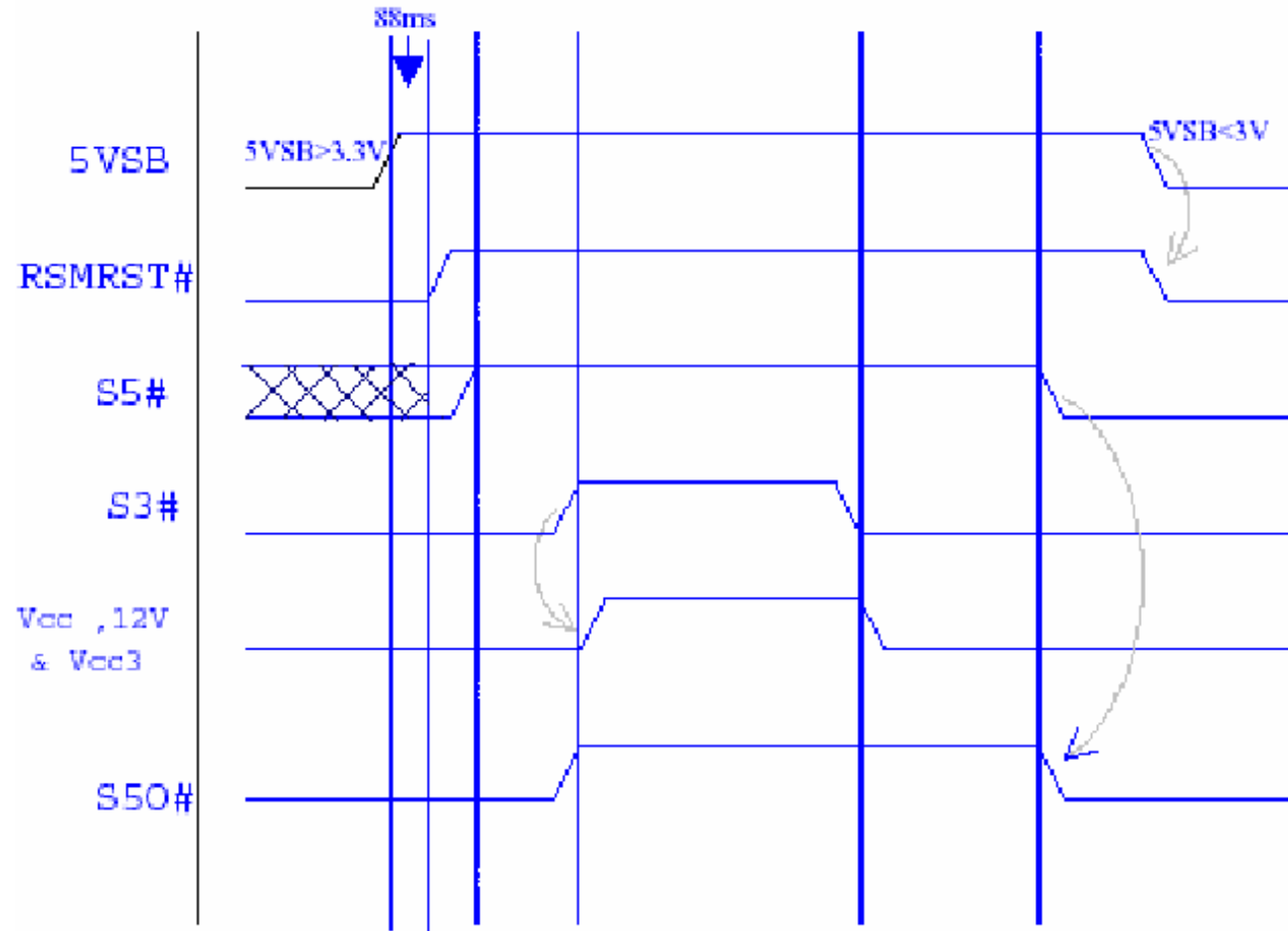
## VCC VID / VID\_GOOD



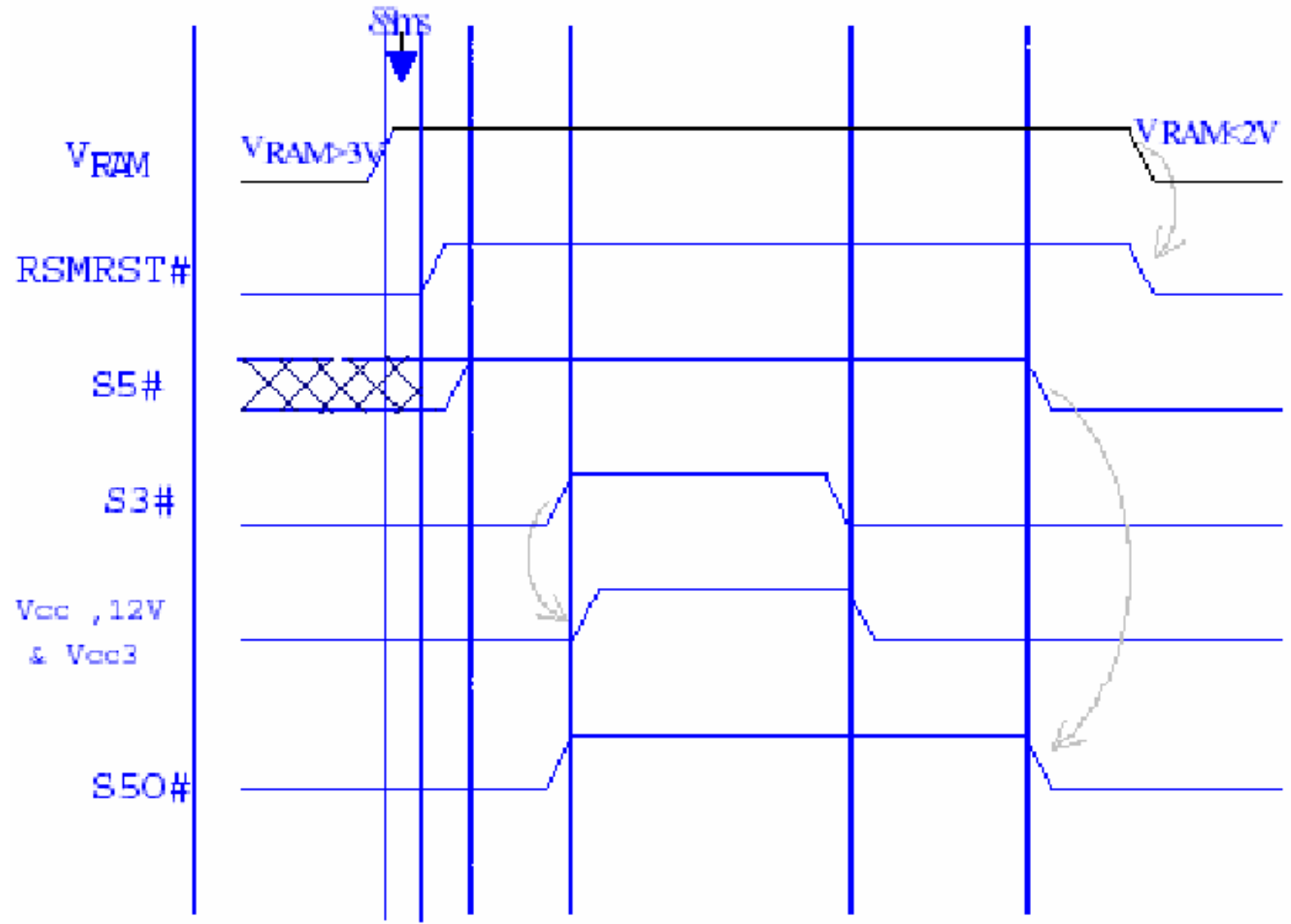
## DDR 2.5V Power



# SYSTEM Power Sequence (S1=L)

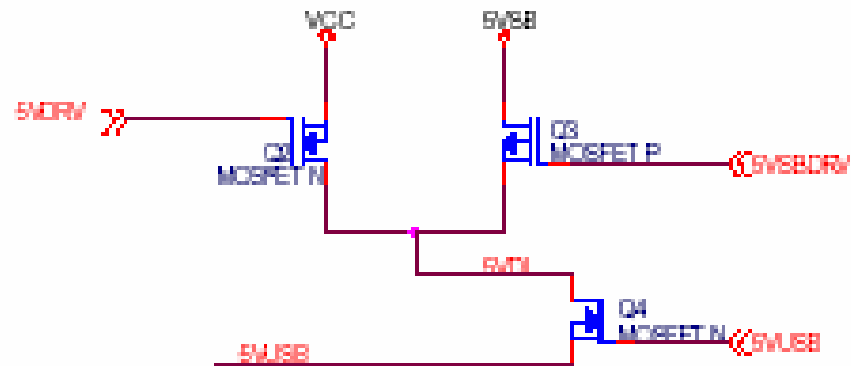


# SYSTEM Power Sequence (S1=H or Tri-state)

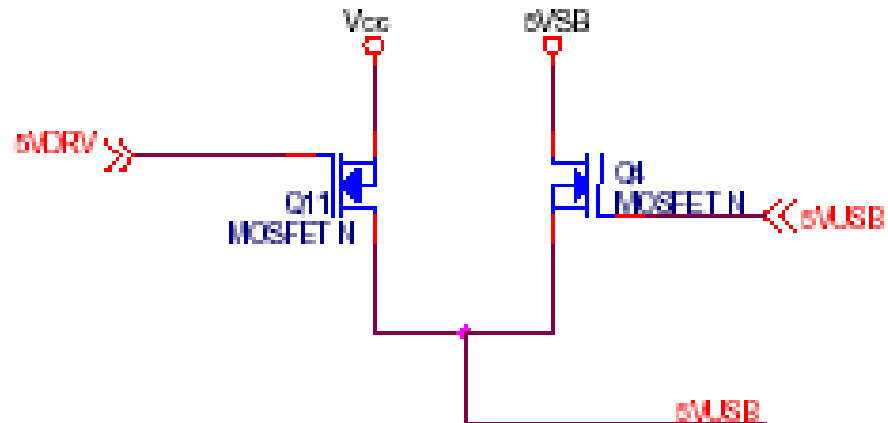


# 5V<sub>DL</sub>/5V<sub>USB</sub> Power Circuit

5V<sub>USB</sub>(1 MOSFET)



5V<sub>USB</sub>(2 MOSFET)

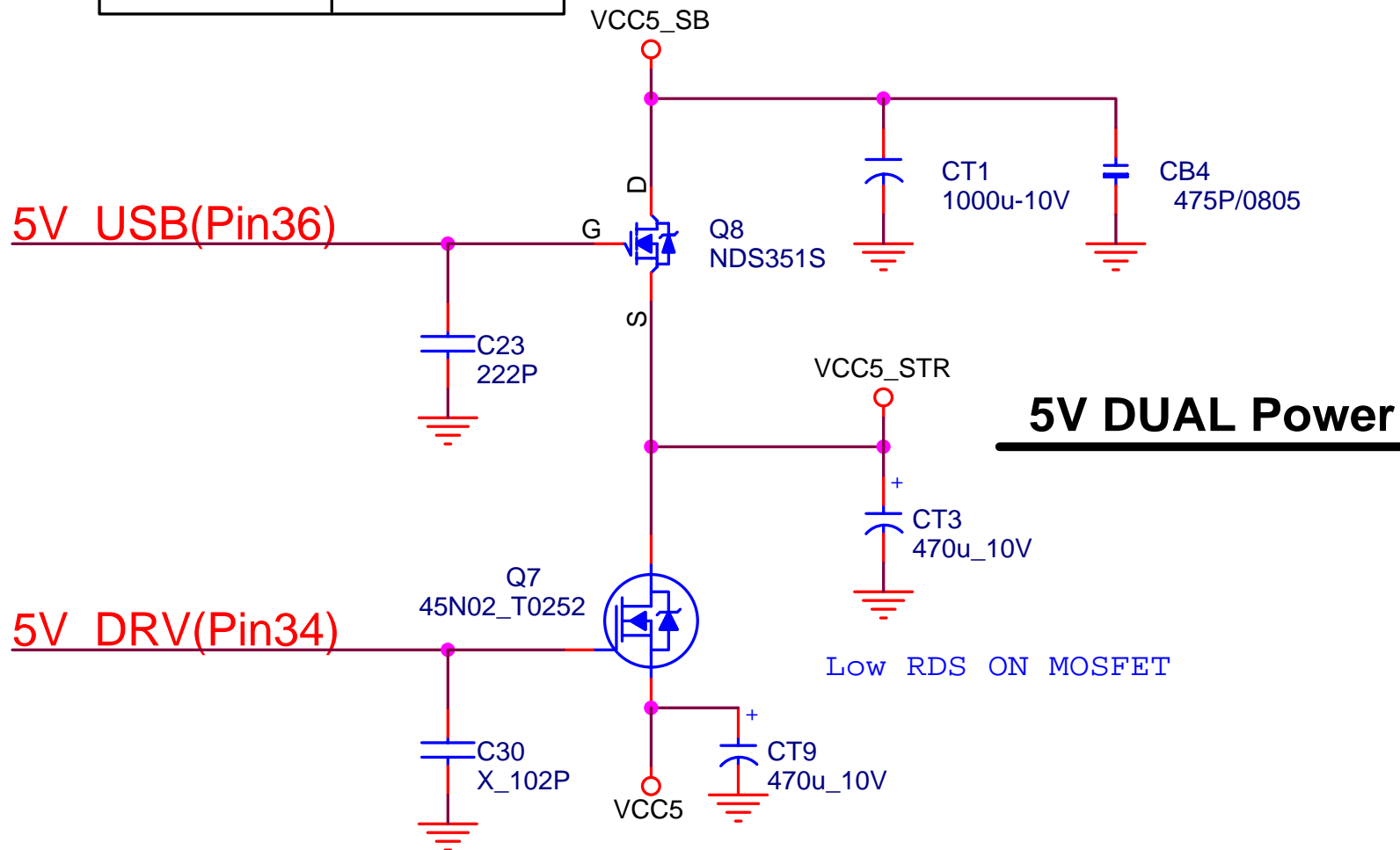


# 5VDUAL Power Circuit

SEL0(Pin37)	5VUSB
H	2 MOSFET
L	1 MOSFET

\*\*S50# pin function(Hi level = 5V)  
same as 5VUSB(Hi level = 12V)

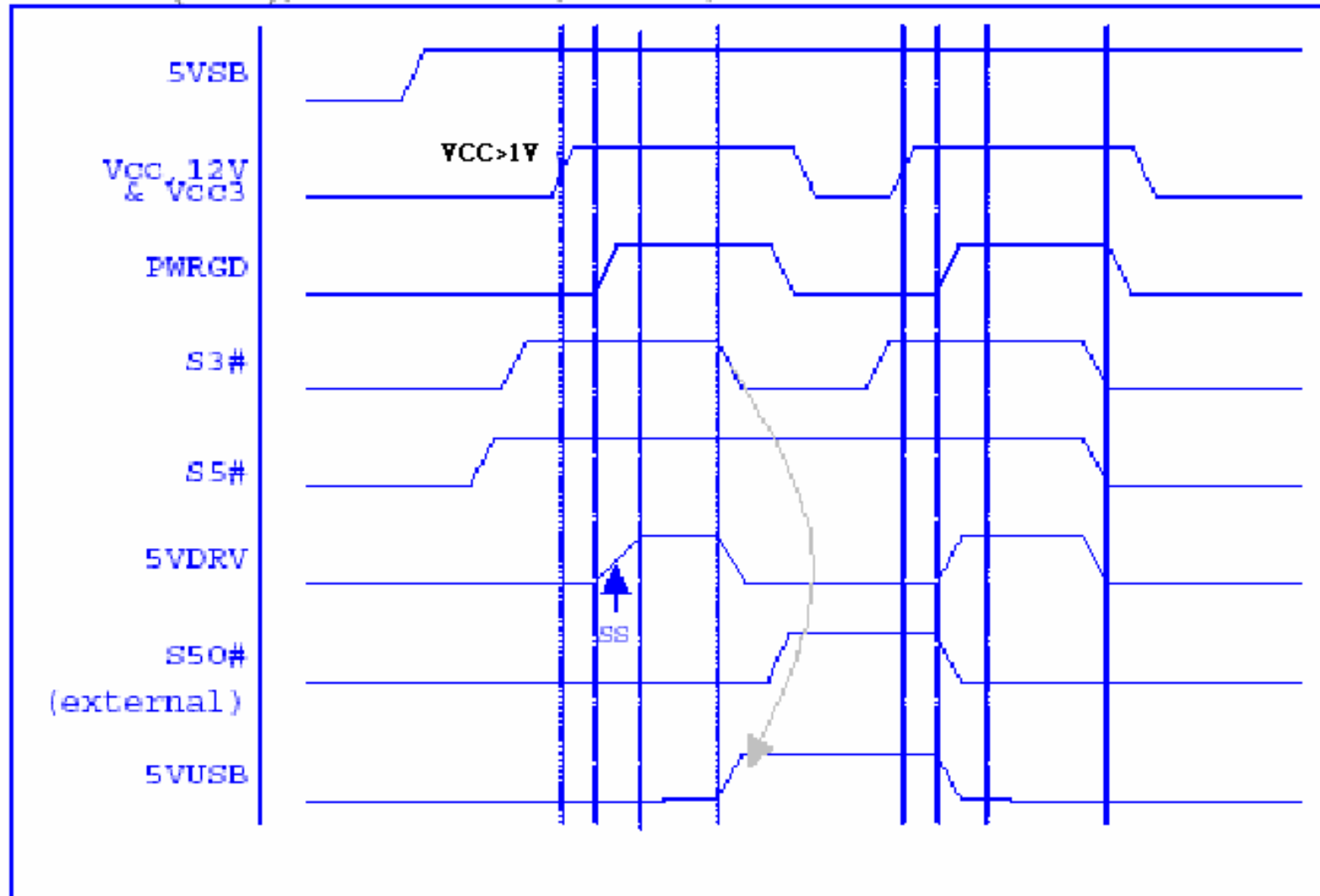
5VUSB USE 2 MOSFET





# 5VDUAL Power Sequence (STR)

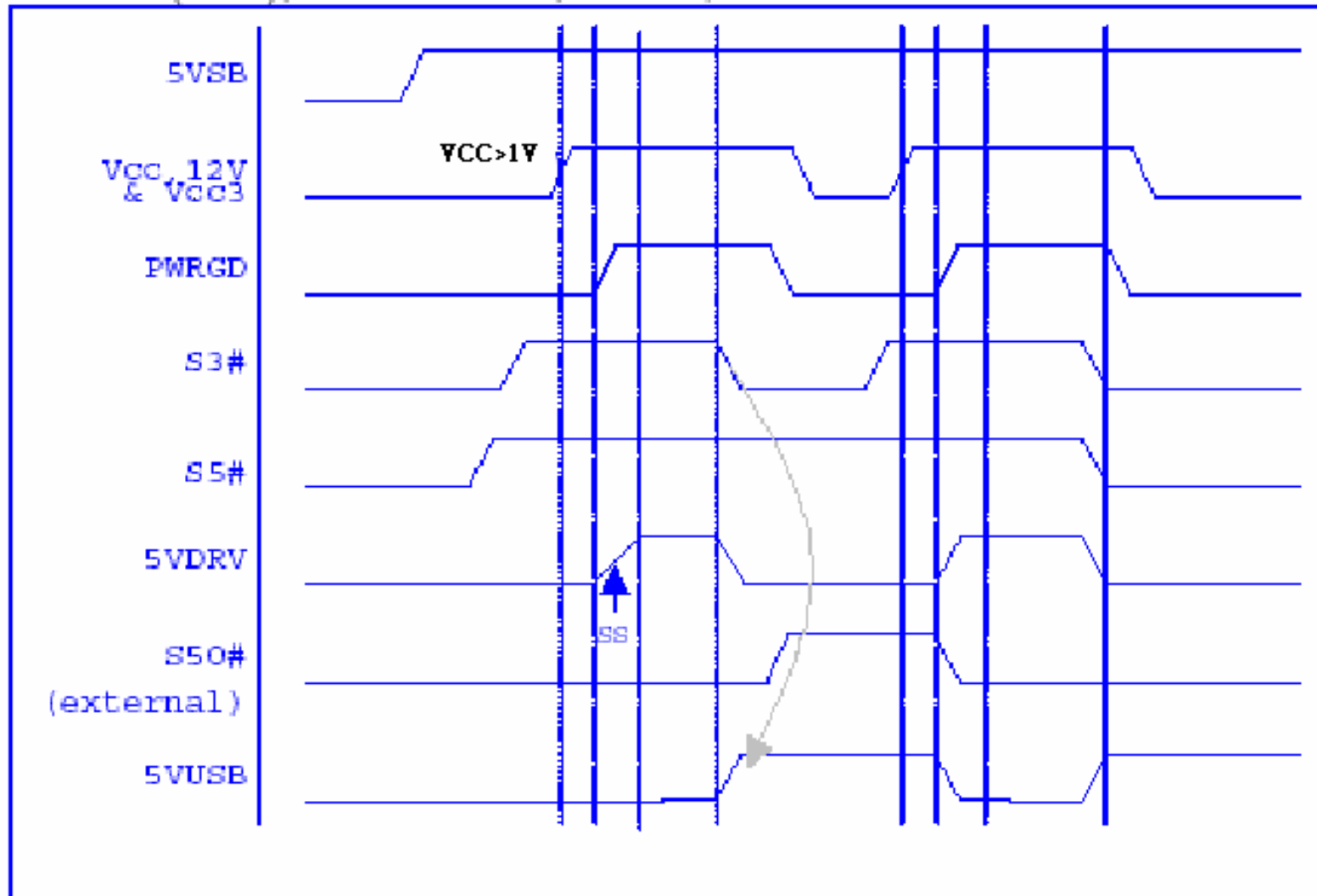
-5VUSB (STR), CR0E Bit0=0 , Bit1=0 , Bit2=1



\*SS (Soft-Start) starts ramp when Vcc arrives to 1V

# 5VDUAL Power Sequence (Dual)

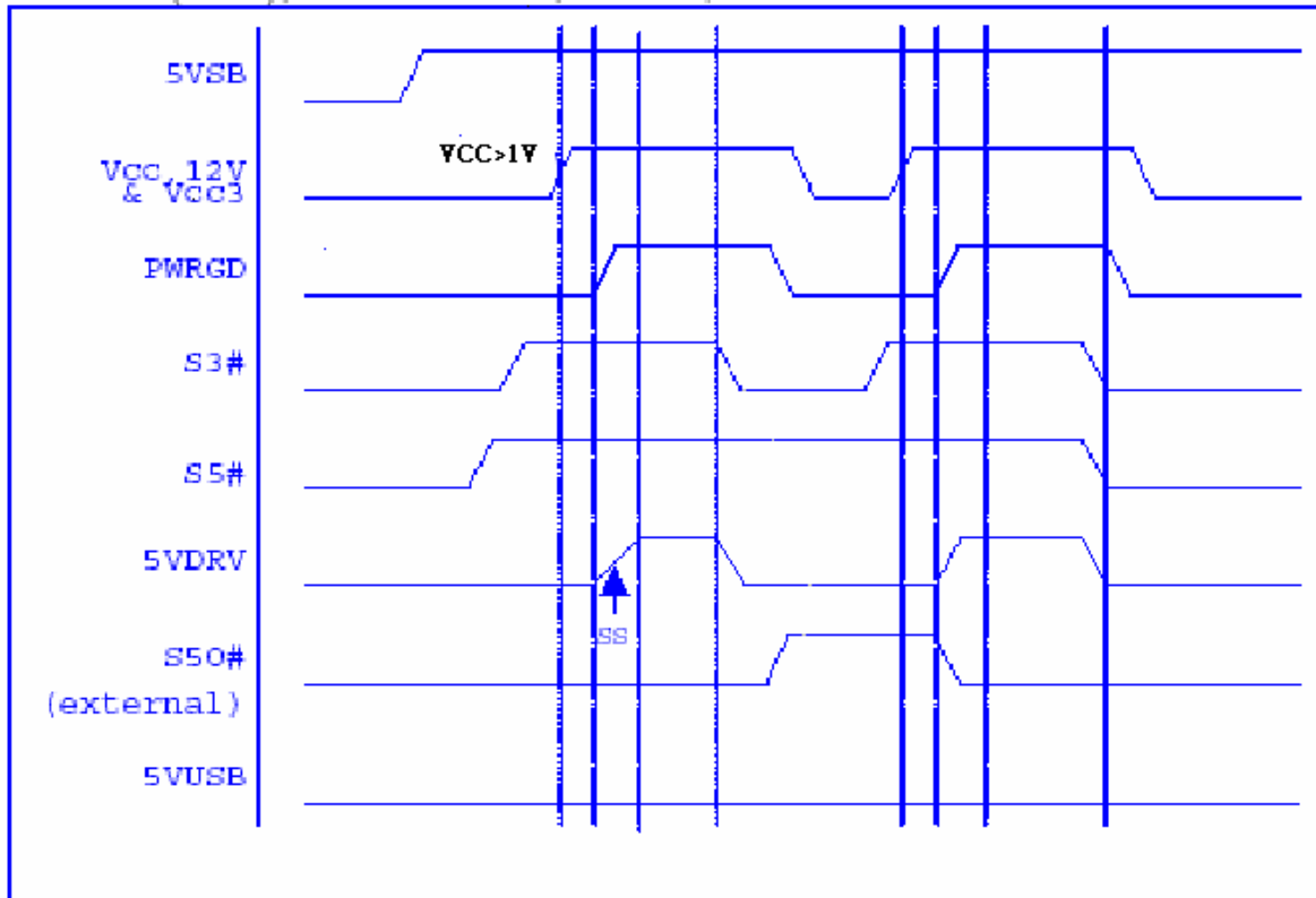
-5VUSB (STR), CR0E Bit0=1, Bit1=0, Bit2=1



\*SS (Soft-Start) starts ramp when Vcc arrives to 1V

# 5VDUAL Power Sequence (5Vcc)

-5VUSB (STR), CR0E Bit0=0 , Bit1=1 , Bit2=1

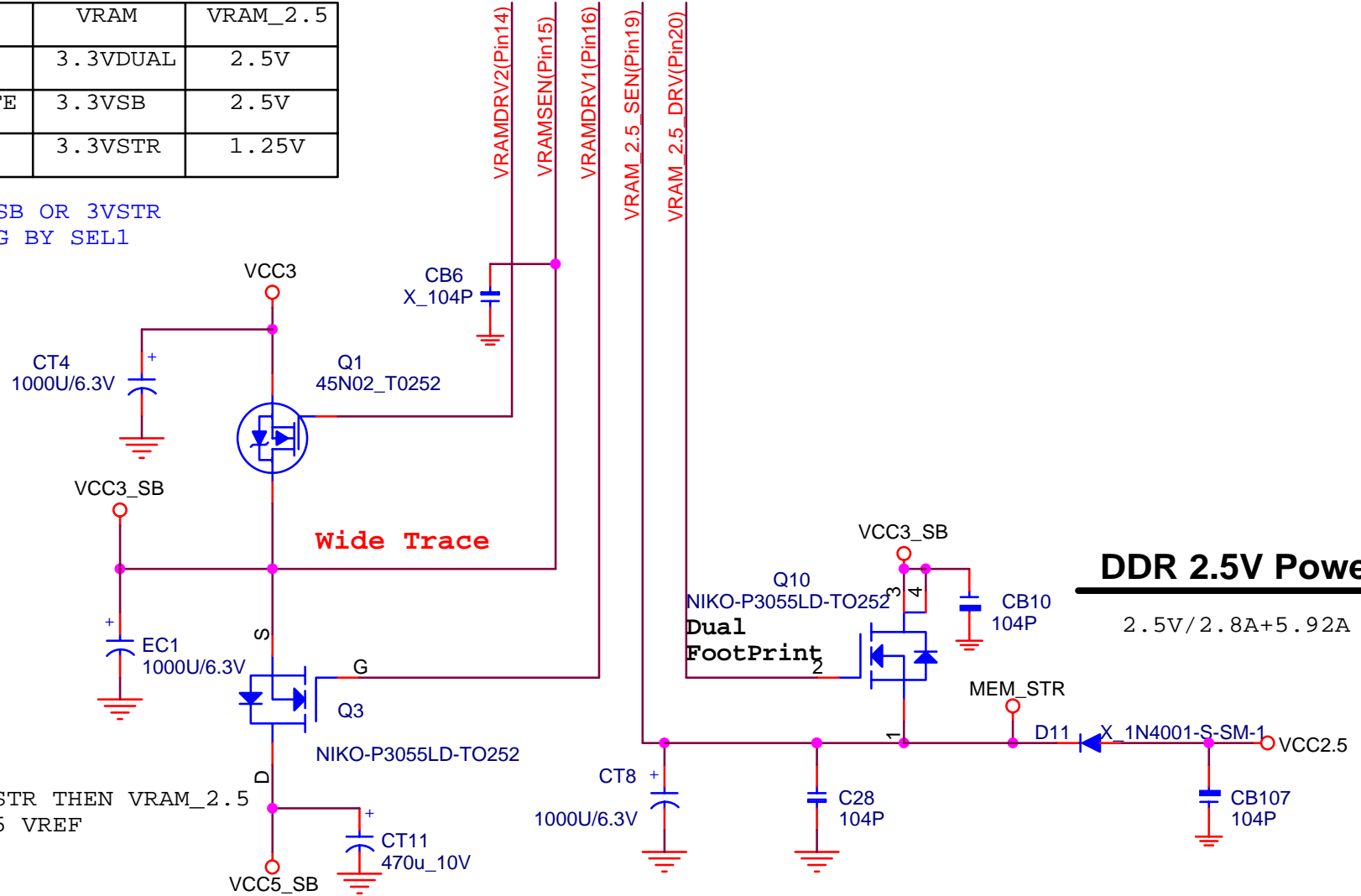


\*SS (Soft-Start) starts ramp when Vcc arrives to 1V

# 3VSB & DDR2.5V Circuit

SEL1	VRAM	VRAM_2.5
H	3.3VDUAL	2.5V
TRI-STATE	3.3VSB	2.5V
L	3.3VSTR	1.25V

FOR 3VSB OR 3VSTR  
SETTING BY SEL1



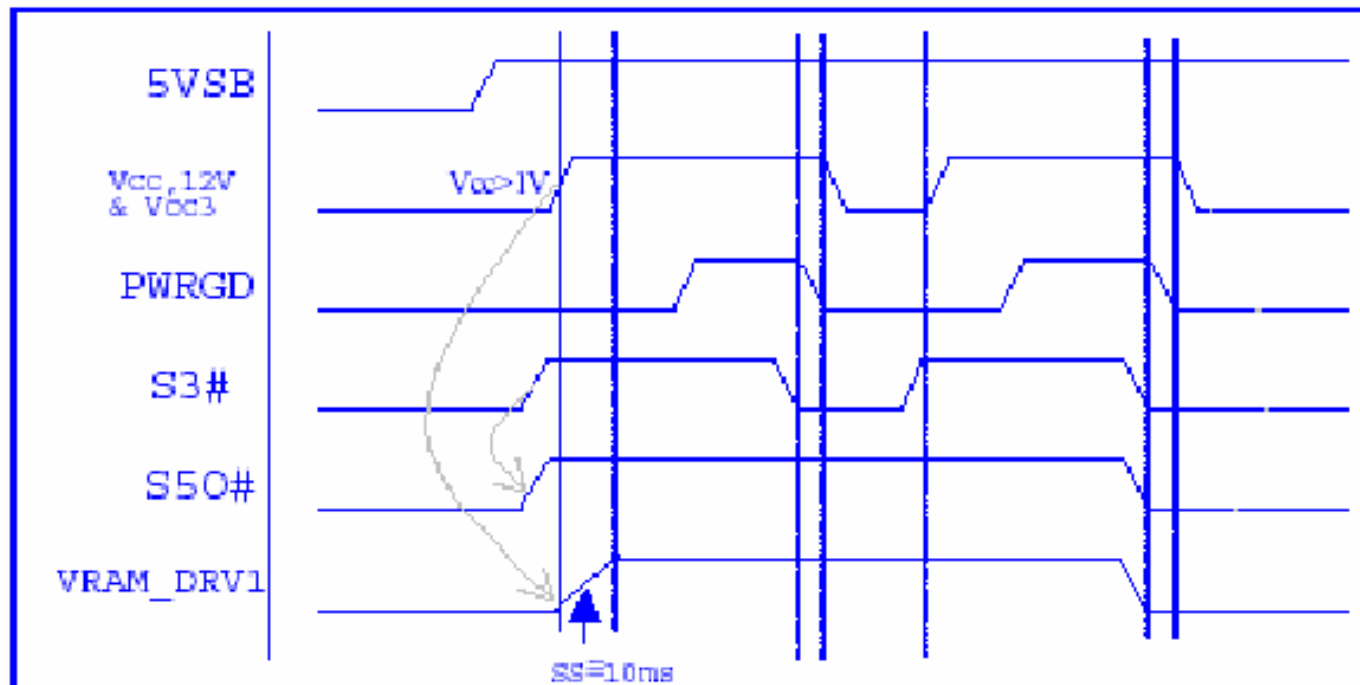
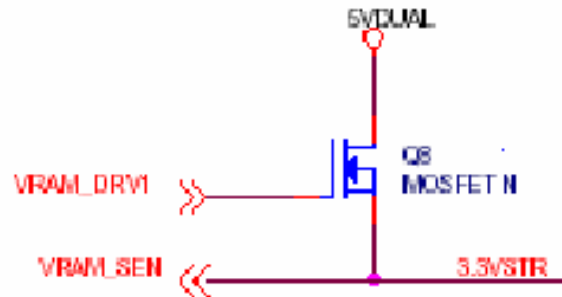
## DDR 2.5V Power

2.5V / 2.8A + 5.92A

\*\* SETTING 3VSTR THEN VRAM\_2.5  
BECOME TO 1.25 VREF

# 3VSB Power sequence (S1=0, 3.3VSTR)

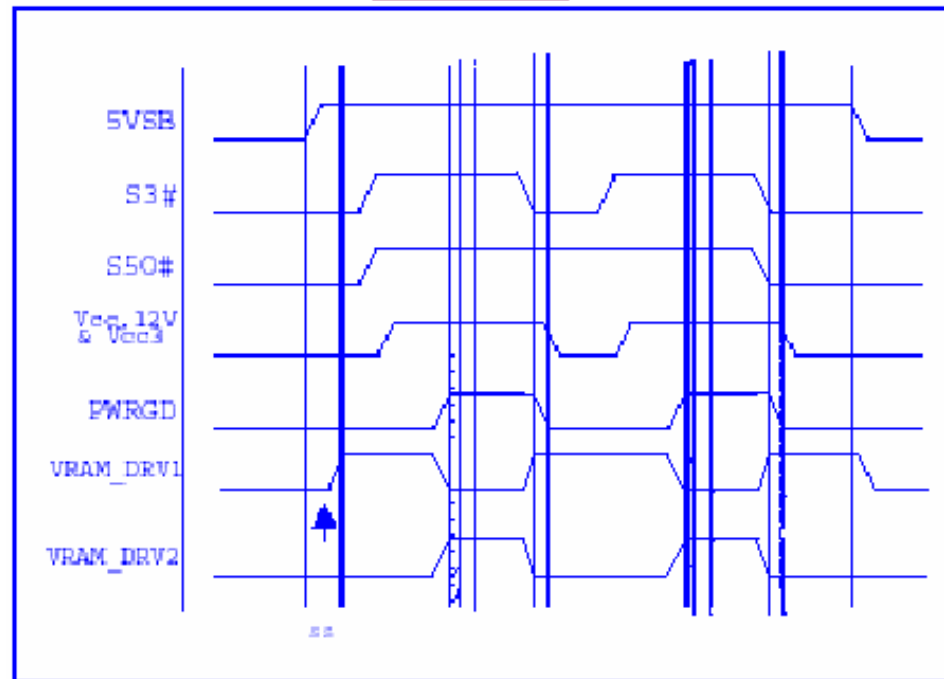
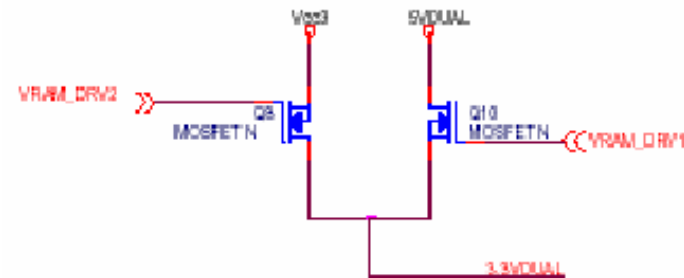
$V_{RAM}$  (S1=0):



SS (Soft-Start) starts ramp when Vcc arrives to 1V

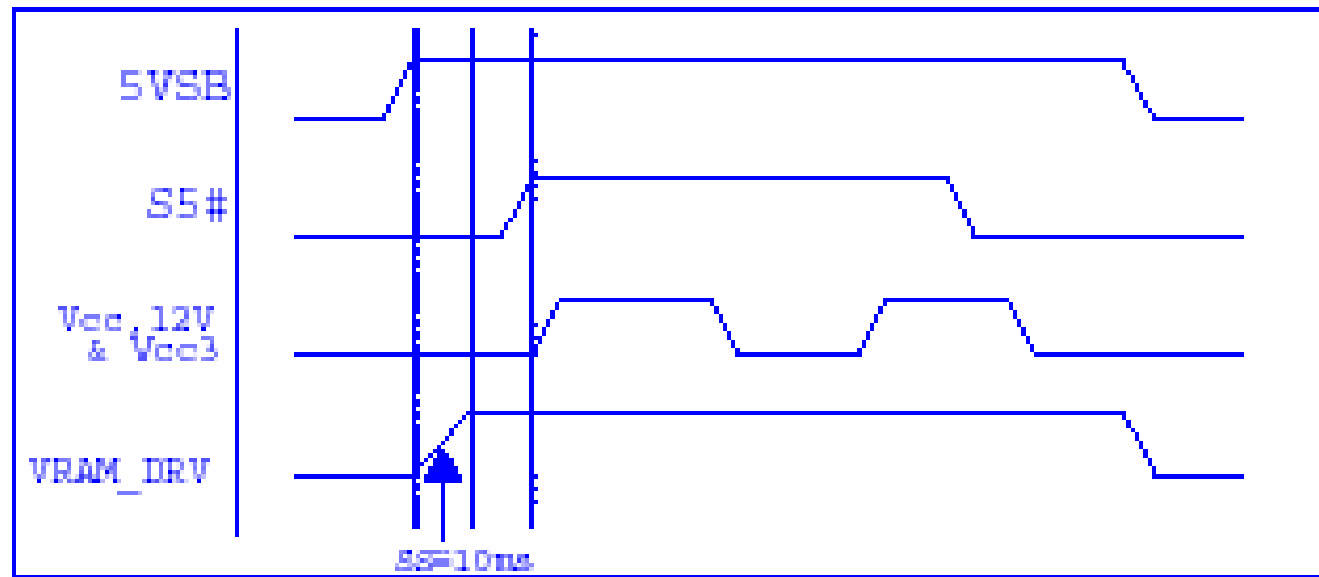
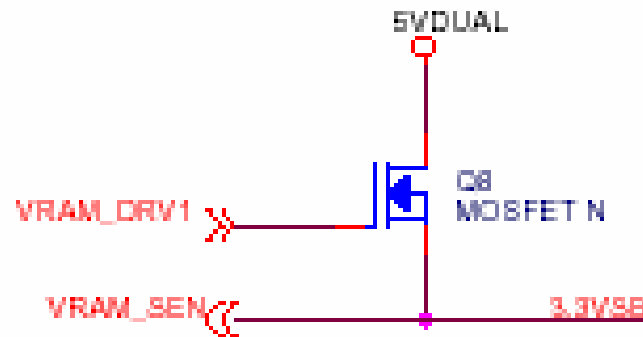
# 3VSB Power sequence (S1=1, 3.3VDUAL)

V<sub>RAM</sub> (S1=1)



# 3VSB Power sequence (S1=Tri-state, 3.3VSB)

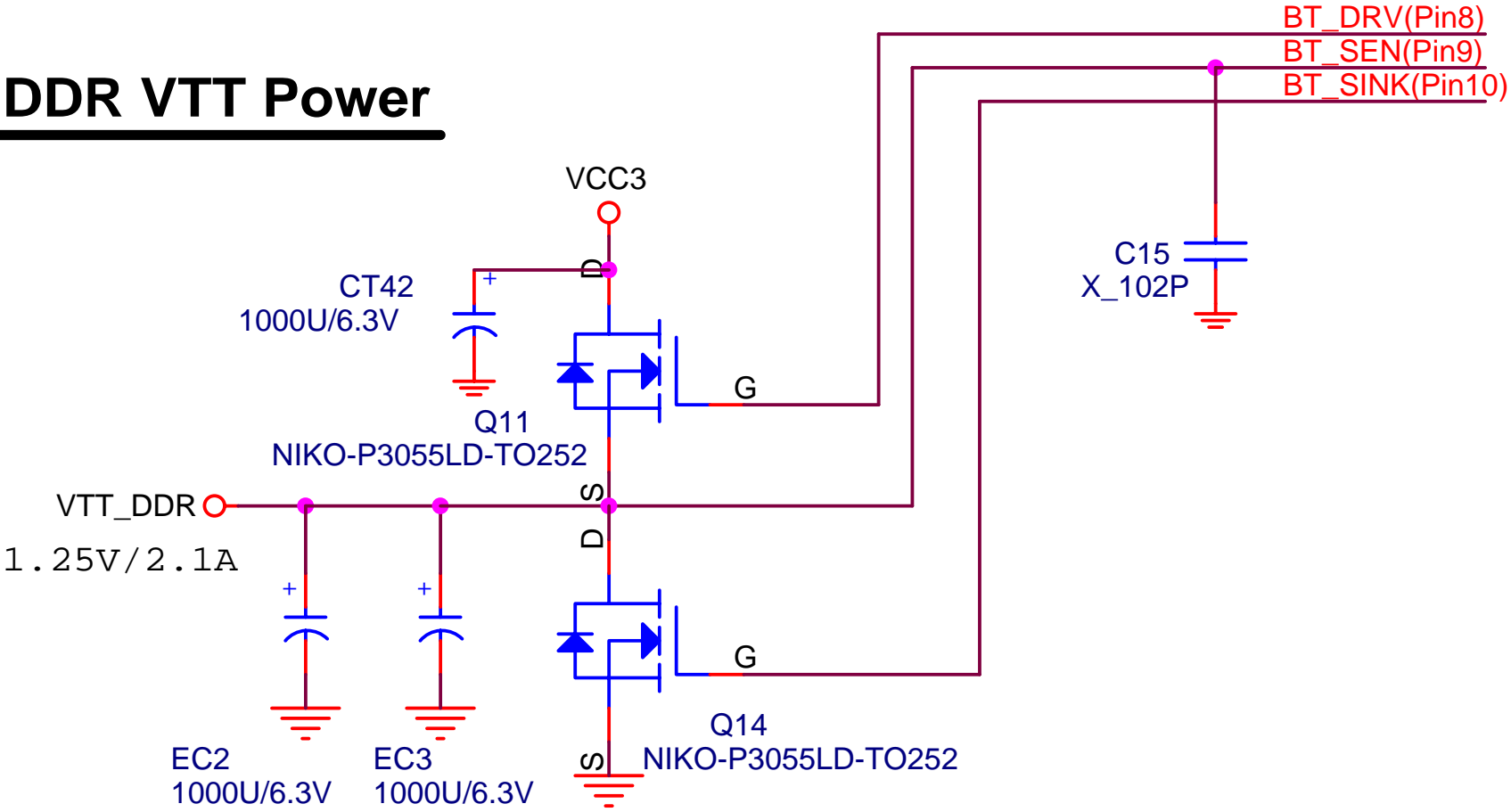
$V_{RAM}$  (S1=Tri-state)



\*SS (Soft-Start) starts ramp when 5VSB arrives to 4V

# DDR VTT Circuit

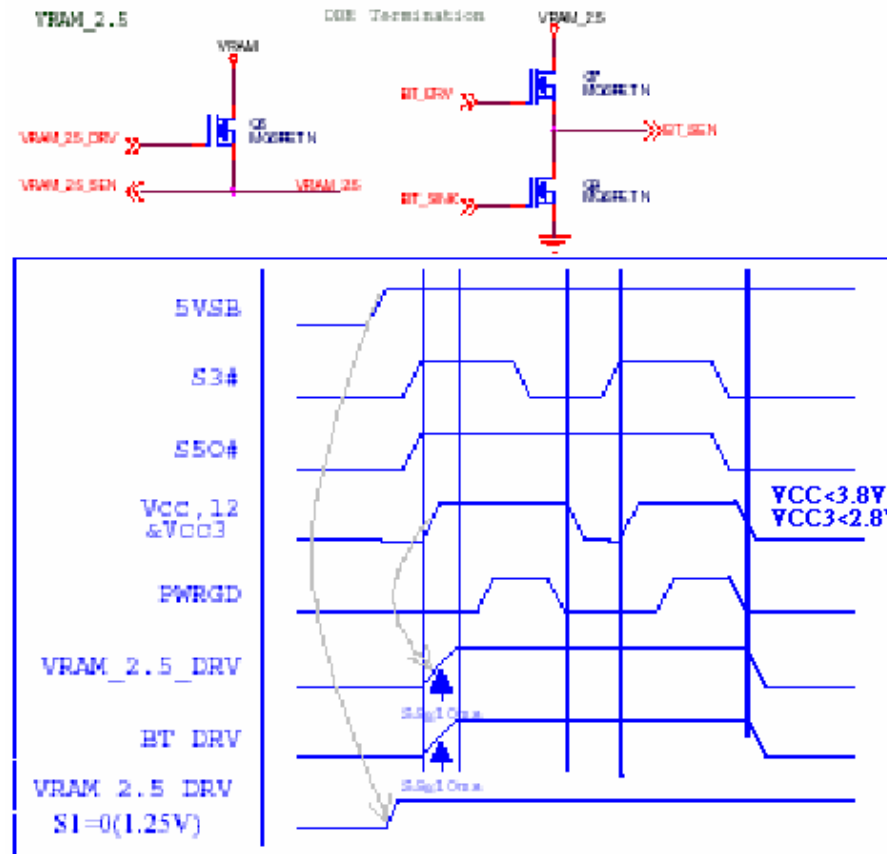
## DDR VTT Power





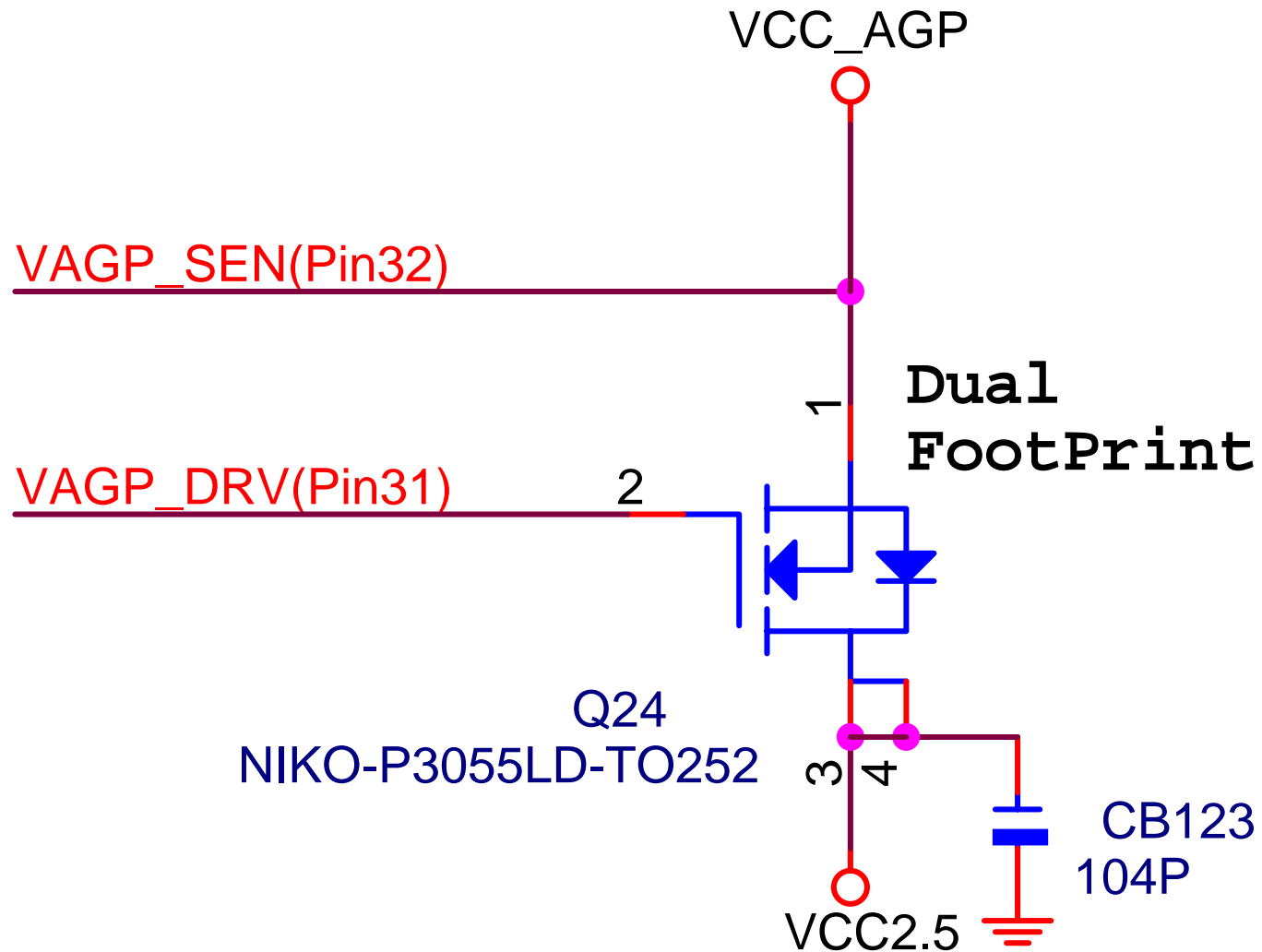
# VRAM\_2.5 and DDR Termination V<sub>BT</sub> power sequence

VRAM\_2.5 & DDR Termination V<sub>BT</sub>



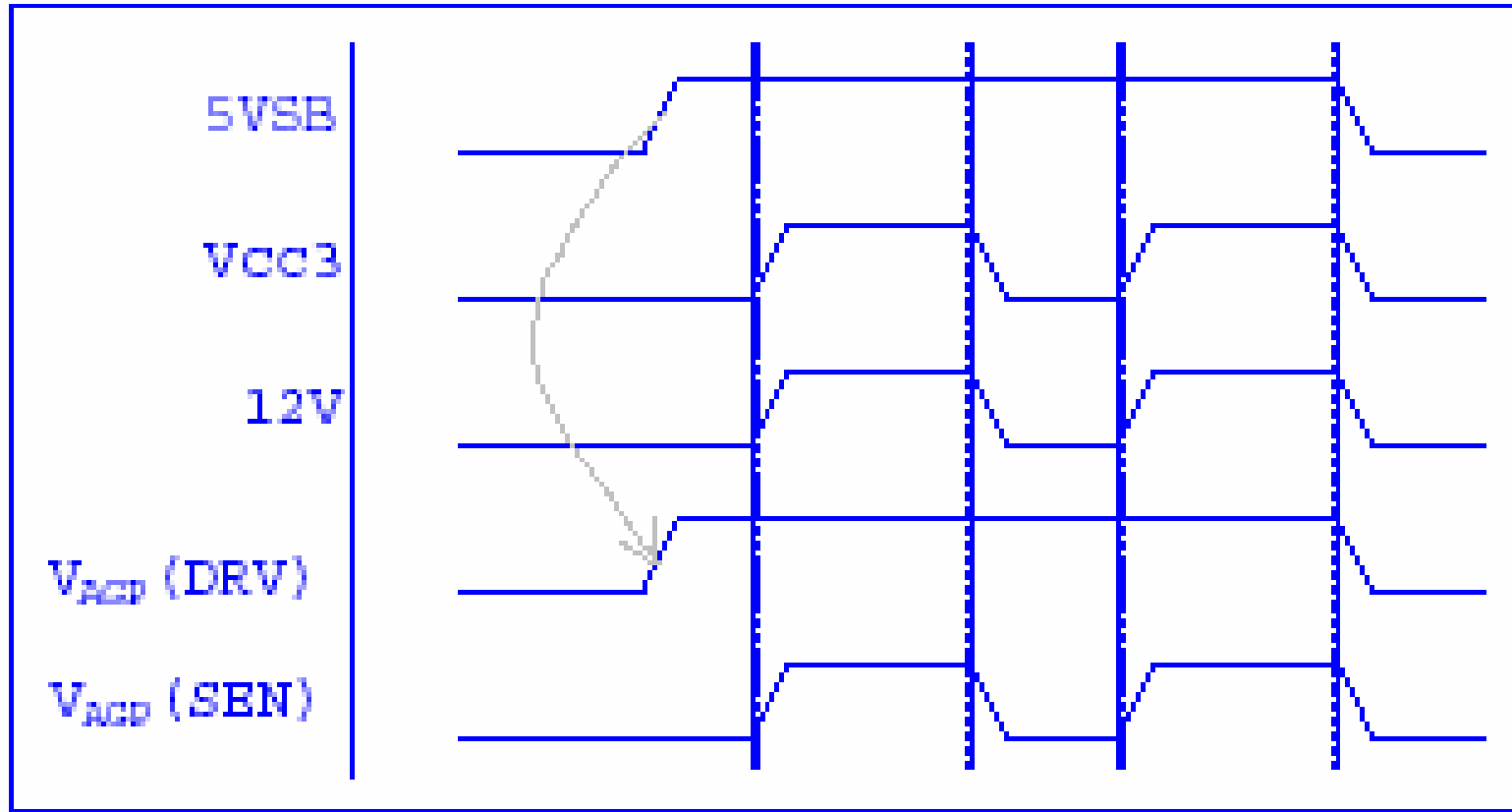
\*SS (Soft-Start) starts ramp when Vcc arrives to 1V

# VCC\_AGP Circuit [TYPEDET#(Pin33)=0]

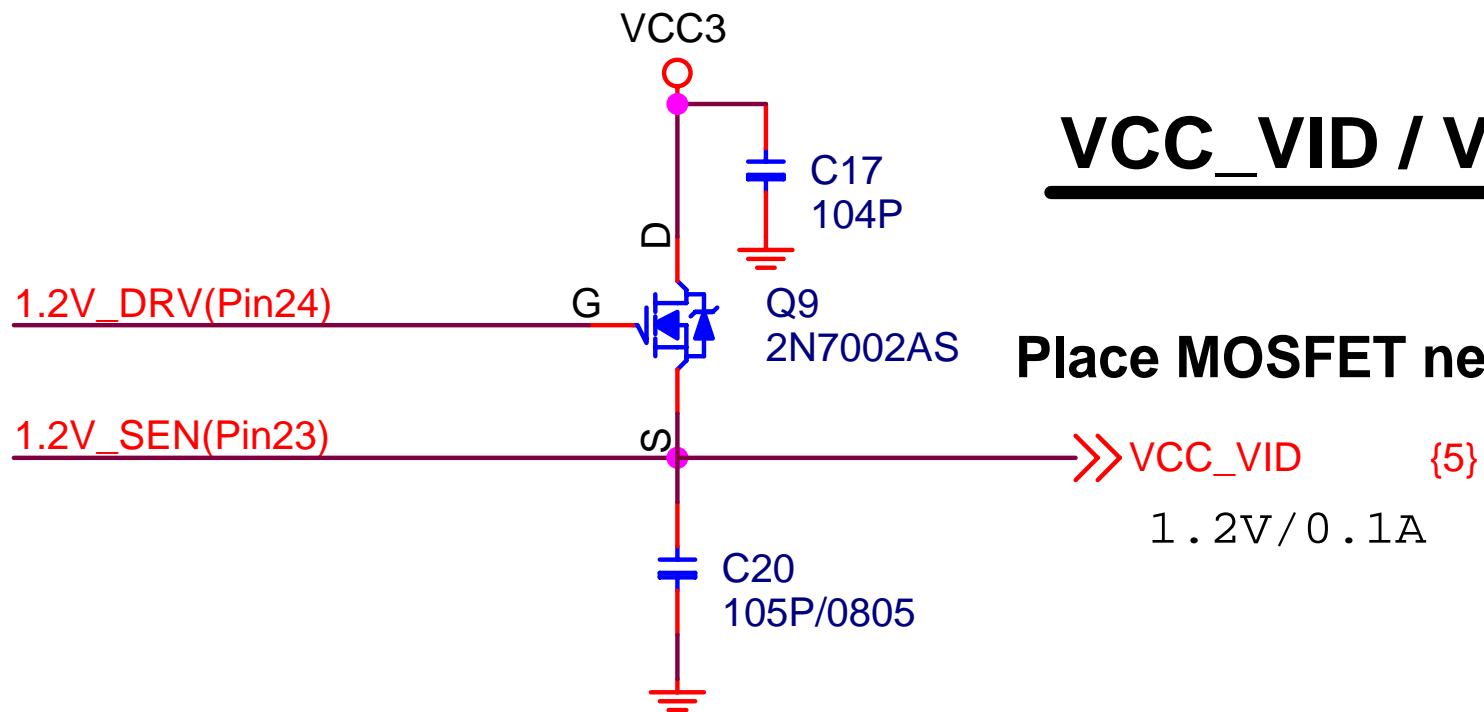


# VCC\_AGP Power Sequence

$V_{AGP}$ :



# VCC\_VID Circuit



**VCC\_VID / VID\_GOOD**

**Place MOSFET near CPU**

# VCC\_VID Power Sequence

1.2V for Northwood or Tualatin CPU

